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A Novel Seven Level H-Bridge Inverter for Photovoltaic System

[1]S.Selvakumar ,[2]A.Vinothkumar , [3]M.Vigneshkumar
[1]M.E.,(Power Electronics & Drives) [2,3](Assistant Professor Dept of EEE)
P.A College of Engineering & Technology
Pollachi -642002

Abstract
There is strong trend in the photovoltaic (PV) inverter technology to use transformer less topologies in order to acquire higher efficiencies. The general function of multilevel inverter is to synthesis desired voltage from solar source. This inverter has advantageous of industrial applications. The use of converters will increase losses and cost in conventional methods. The proposed seven level multilevel inverter with solar energy using Pulse Width Modulation Technique (PWM) of providing high switching frequency will highly reduce harmonics. The inverter produces output voltage in seven levels V_{dc}, $V_{dc}/3$, $2V_{dc}/3$, 0,$-V_{dc}/3$,$-2V_{dc}/3$,$-V_{dc}$. The validity of the propose inverter is verified through simulation.

Keywords:*Pulse Width Modulation (PWM), Photovoltaic (PV) Source, Maximum Power Point (MPP).*

I. Introduction

The PV inverter, which is the heart of a PV system, is used to convert dc power obtained from PV modules into ac power to be fed into the load.Improving the output waveform of the Inverter reduces its respective harmonic content and, hence, size of the filter used and the level of the Electromagnetic Interference (EMI) generated by switching operation of the inverter. In recent years, multilevel inverters have become more attractive for researchers and manufacturers due to their advantages over conventional three level PWM Inverters. They offer improved output waveforms, smaller filter size and lower EMI, lower Total Harmonic Distortion (THD). A multilevel inverter has several advantages over a conventional two-level converter that uses high switching frequency Pulse Width Modulation (PWM). The attractive features of a multilevel inverter can be briefly summarized as follows. 1). Staircase Waveform Quality: Multilevel inverters not only can generate the output voltages with very low distortion, but also can reduce the dv/dt stresses; therefore Electro Magnetic Compatibility (EMC) problems can be reduced. 2) Common-Mode (CM) Voltage: Multilevel inverters produce smaller Common mode voltage; so that stress in the bearings of a motor get reduced which is connected to the multilevel inverter. Furthermore, CM voltage can be eliminated by using advanced modulation strategies. 3) Input Current: Multilevel inverters can draw input current with low distortion. 4) Switching Frequency: Multilevel inverters can operate at both fundamental switching frequency and high switching frequency PWM [12].

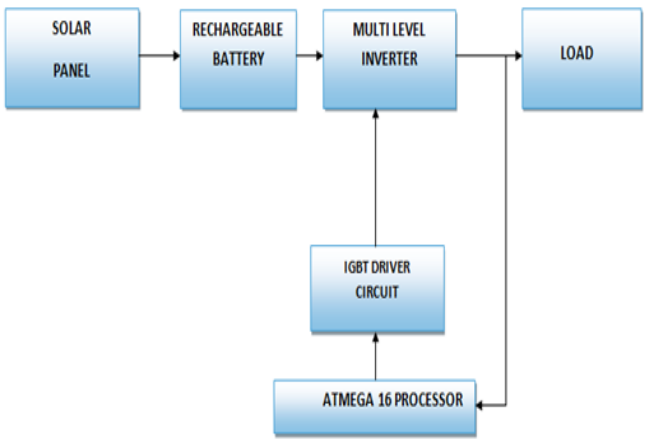


Fig.1. Block Diagram of the Proposed Model

The inverter generates 2^{s+1}-1 different voltages (e.g. an inverter with s=2 cells can generate 2^3-1=7 different voltage level).In conventional method low level inverter is used and better sinusoidal waveform was not obtained which is the drawback of the conventional system and the harmonics was high. So increasing the levels of inverter to get high resolution, hence the output waveform is mostly sinusoidal waveform [8].In conventional method, some additional drawbacks like electromagnetic compatibility and common mode voltage problems easily occurs consuming large current cause swing in the voltage due to harmonics which can be easily viewed by our vision . Example: rolling lines in Television using inverters.

II. Circuit Description of The Proposed System

The hybrid cascaded H-bridge inverter power circuit is illustrated in Fig.2. The inverter is composed of two legs, in each one a series connection of two H-bridge inverters fed by independent DC sources that are not equal ($V1 < V2$). In this proposed method of the inverter, has two input stages, all the two stages are alike in the construction module. All the modules are connected as new cascaded with each module having power switches. The power switches may be IGBT, MOSFET or any other power devices, IGBT's are used in this system. The power switches are operated in switching mode such that any two switches are in operating conditions at time and other at time and other two switches are in open condition. One switch from upper arm as well as lower arm act in the operating condition of corresponding bridge.

The use of asymmetric input voltages can reduce, or when properly chosen, eliminate redundant output levels, maximizing the number of different levels generated by the inverter. Therefore this topology can achieve the same output voltage quality with less number of semiconductors. This also reduces volume, costs, and losses and improves reliability. When cascading two level inverters like H-bridges, the optimal asymmetry is obtained by using voltage sources proportionally scaled to the two H-bridges power. seven different output levels can be generated using only two cells (8 switches) while three cells (12 switches) are necessary to achieve the same amount of level with symmetric fed inverter.

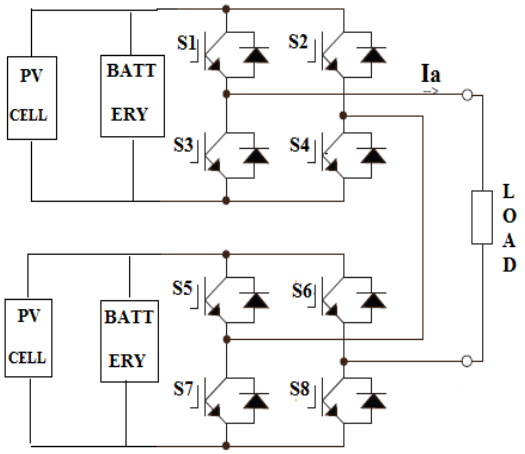


Fig. 2. Circuit Diagram of Multilevel Inverter

III. Switching Pattern

For first pulse, switches one and four V_{dc} will act along with action of switches five and six produce first level of output waveform and after next duration of pulses switches five and eight act to produce 2Vdc along with action of switches three and four produces 0Vdc gives +2Vdc form next level in the output waveform without any distortion. The next pulses of action from IGBT driver circuit make switches of five and eight in the second bridge of power circuit to produce +2Vdc along with action of switches one and four gives +3Vdc output waveform. After the completion of the third level output waveform the control pulses ready to produce next stage of output waveform by making switches two and three gives $-V_{dc}$ along with action of switches five and eight in the second bridge gives $-2V_{dc}$ gives fifth level of output waveform with resolution of high switching frequency which reduces the harmonics in the output waveform to obtain pure supply to load.

Table 1.Active Switching Pattern

S.no	S1	S2	S3	S4	S5	S6	S7	S8	O/P V_{dc}
1	1	0	0	1	0	0	0	0	+1
2	0	0	1	1	1	0	0	1	+2
3	1	1	0	0	1	1	0	0	+3
4	0	0	0	0	0	0	0	0	0
5	0	1	1	0	0	1	1	0	-3
6	0	0	0	0	0	1	1	0	-2
7	0	1	1	0	1	1	0	0	-1

This process of action keeps on continuing produces corresponding stage of output level form pure stepped sinusoidal output waveform was produced.This process goes on increasing the level number of output waveform to provide harmonic less pure stepped output waveform to load where switching pattern is shown in the Table.1.The main advantage of proposed system is IGBT's were used instead of MOSFET,switches, flying capacitors reduces which will consequently reduce gate triggering losses,switching losses.

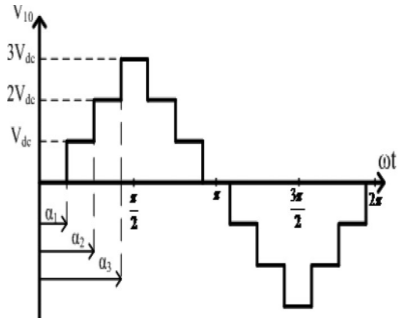


Fig.3. Switching Pattern of Seven Level Inverter

The S number of stages or DC source and the associated number output level can be written as follows:

$$N \text{ level} = 2^{s+1}-1 \quad (1)$$

The number of switches used in this topology is expressed as,

$$N \text{ Switches} = 4S \quad (2)$$

Table 2.Step By Step Output Voltage Waveform

Level	**Reaction of H-Bridges to the Control Pulses**					**Waveform Generation**
	Bridge1 1Vdc	**Switches**	**Bridge 2 2Vdc**	**Switches**	**O/P Vdc**	
1	**+1**	**1,4**	**0**	**5,6**	**+1**	
2	**0**	**2,3**	**+2**	**5,8**	**+2**	
3	**+1**	**1,2**	**+2**	**5,8**	**+3**	
4	**0**	**3,4**	**0**	**7,8**	**0**	
5	**-1**	**2,3**	**-2**	**6,7**	**-3**	
6	**0**	**3,4**	**-2**	**6,7**	**-2**	
7	**-1**	**2,3**	**0**	**5,6**	**-1**	

IV. Characteristics Of Pv Cells

a. Characteristics of PV cell at Constant Temperature

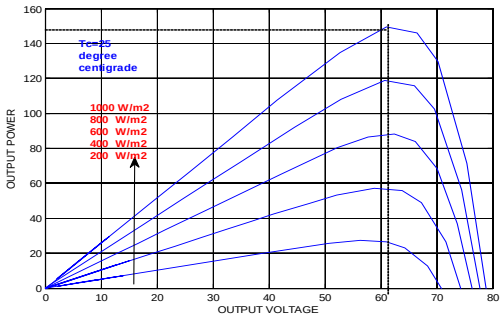


Fig.4. Power and voltage waveform at constant temperature for PV cells

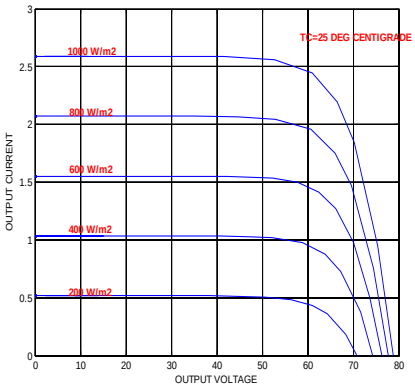


Fig.5. Power and Voltage Waveform at Constant Irradiance for PV cell

b. Characteristics of PV cell at constant irradiance

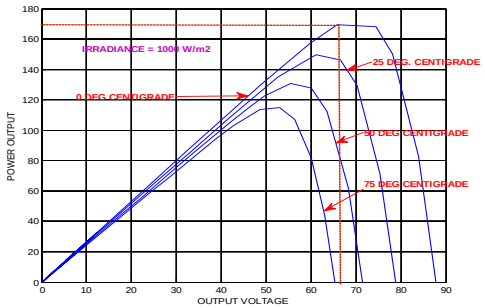


Fig.6. Power and Voltage waveforms at Constant Irradiance for PV cell

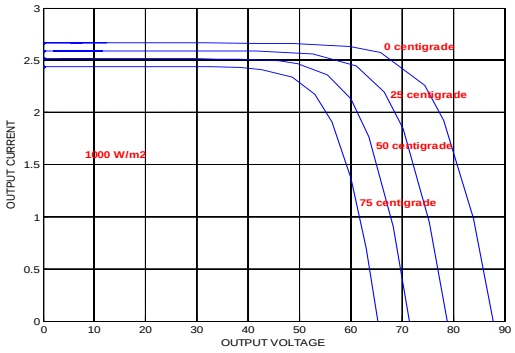


Fig.7. Current and Voltage waveform at Constant Irradiance for PV cells

From the above characteristics (Fig.4, Fig.5, Fig.6, Fig.7) curves the power generation continuously varies along with two main factors, which are known as cell temperature and irradiance. In this work MPPT technique is used for finding the maximum output at various instant of time.

V. Simulink Model Of Seven Level Inverter

The feasibility of the proposed approach is verified using computer simulations. A model of the seven-level inverter is constructed in MATLAB-Simulink software. A new strategy with reduced number of switches is employed. Cascaded 7 level inverter requires 12 switches to get seven level output voltage and with the proposed topology requirement is reduced to 8 switches. The new topology has the advantage of its reduced number of switching devices (switches) compared to conventional cascaded H-bridge multilevel inverter, and can be extended to any number of levels.

The below simulink model in Fig.8 could recreate the characteristic curves shown in Fig.6 and Fig.7 . The life time of the PV panel depends on the environmental conditions at which the panel is installed. Ageing effect is unavoidable but it can be minimized using anti-aging agents like ethylene vinyl acetate. This serve to improve the life time of PV panel to certain extent. The exact life time of the PV panel is unpredictable as it depends upon the field conditions and quality of manufacturing.

A) *Simulation Diagram of Multilevel Inverter*

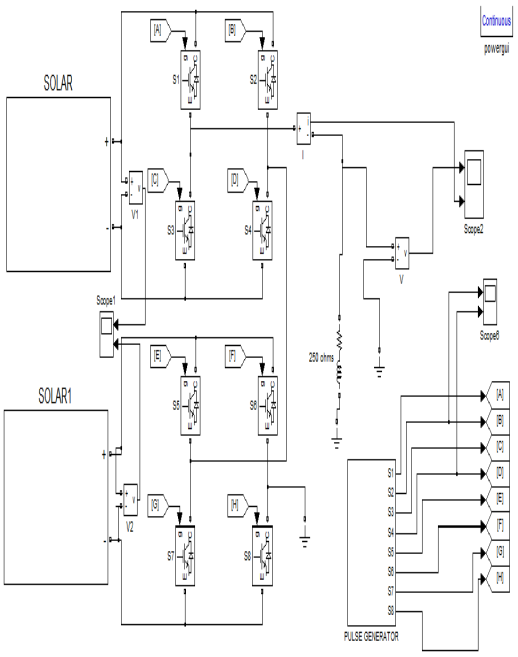


Fig 8. Simulink Model of Seven level Inverter

VI. COMPARISION OF PROPOSED SYSTEM WITH SOLAR SOURCE AND SEPARATE DC SOURCE

Table 3. Level Description

	Proposed System with solar source	**Existing separate Dc source MLI**
No of levels S=No of stages S=2	2^{s+1}-1 7 level	2s+1 7 level
Input DC voltage	V dc 2vdc	1Vdc 1Vdc 1Vdc

The efficiency of the proposed system is higher than a conventional inverter for applications where switching losses are high. Reduced numbers of switches were used in the proposed solar based MLI. It is an attractive solution to get large number of levels together with a better efficiency.

VII. Results And Discussions

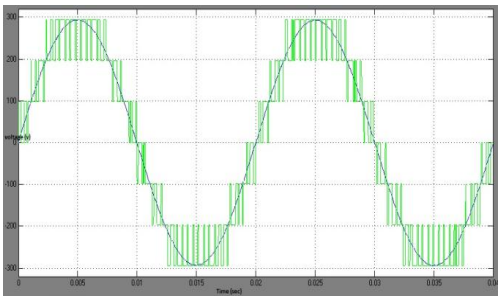
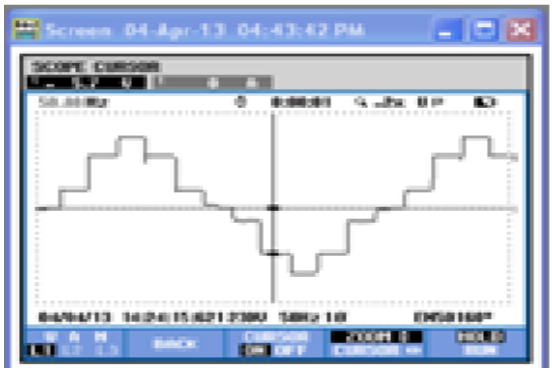
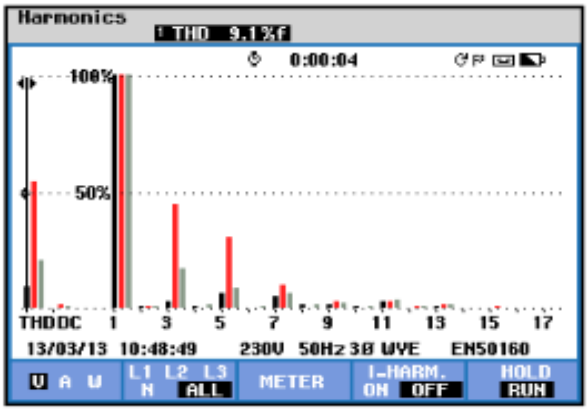


Fig.9. Simulation of Seven Level Inverter Output voltage $(M \leq 0.5)$

(a)



(b)



(c)

Fig 10. Experimental Setup

It is fact that harmonic components in load current closely affect the performance of the existing inverter The (THD) is one of these measures, which evaluates the quantity of harmonic contents in the output waveform and is a popular performance index for power inverters. Fig 9. Shows simulink output of seven level inverter. Fig 10. (a),(b),(c) shows the hardware set up and outputs measured by Power Quality Analyser. The Percentage of harmonics obtained is 9.17%.From the above result proposed system gives high efficiency.

VIII. CONCLUSION

Asymmetrical multilevel inverter topology has been proposed in our work. The most important thing of the proposed system is being convenient for expanding and increasing the number of output levels simply with less number of switches. This method results in the reduction of the number of switches, losses and cost of the inverter. If we presented hybrid switching, the multilevel inverter generates near-sinusoidal output voltage and as a result, very has low harmonic content.

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APPENDIX

SIMULINK MODEL OF PV CELL

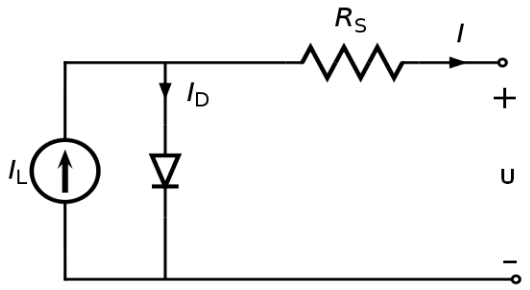

Fig.3 Line Diagram of PV Cell

$$I = I_L - I_D$$

Where,

I = Output Current in Amps

I_L = Photo Generated Current in Amps

I_D = Diode Current in amps

By Shockley equation, current diverted through diode is,

$$I_D = I_o\left[\exp\left(\frac{U + IR_s}{nkT/q}\right) - 1\right] \quad (3)$$

where,

I_o = Reverse Saturation Current

n = Diode Ideality Factor

k = Boltzmann's Constant

T = Absolute Temperature

q = Elementary Charge

For silicon of 25^0C nkT/q =0.0259 volts=α,

$$I_D = I_o\left[\exp\left(\frac{U + IR_s}{\alpha}\right) - 1\right] \quad (4)$$

Substituting above equation in equation (3) we get,

$$I = I_L - I_o\left[\exp\left(\frac{U + IR_s}{\alpha}\right) - 1\right] \quad (5)$$

Where
$\alpha = nkT/q$ is known as Thermal voltage timing completion factor.

Photo generated current I_L is calculated by

$$I_L = \frac{\phi}{\phi_{ref}}\left[I_{L,ref} + \mu_{I,SC}\left(T_c - T_{c,ref}\right)\right] \quad (6)$$

where,

ϕ = Irradiance (W/m^2)

ϕ_{ref} = reference irradiance ($1000\,W/m^2$)

$I_{L,ref}$ = Light current at reference condition

T_c = PV cell temperature

$T_{c,ref}$ = Reference temperature

$\mu_{I,SC}$ = Temperature coefficient of the short circuit current (A/^{0} C)

Saturation Current I_o is given by

$$I_o = I_{o,ref}\left(\frac{T_{c,ref} + 273}{T_c + 273}\right)^3 \exp\left[\frac{e_{gap}N_s}{q\alpha_{ref}}\left(1 - \frac{T_{c,ref} + 273}{T_c + 273}\right)\right] \quad (7)$$

Where,

$I_{o,ref}$ = saturation current at the reference condition (A)

e_{gap} = band gap of the material (1.17eV for Si)

N_s = number of cells in series of the PV module

q = charge of the electron

α_{ref} = value of α at the reference Condition

Thermal Model of Photovoltaic Cell is

$$C_{pv}\frac{dT_c}{dt} = k_{in,pv}\phi - \frac{U \text{ x I}}{\text{A}} - K_{loss}\left(T_c - T_a\right) \quad (8)$$

Where,

C_{pv} = overall heat capacity of PV cell/Module

$k_{in,pv}$ = transmittance absorption product of PV cells

K_{loss} = overall heat loss coefficient

T_a = ambient temperature

A = effective area of PV cell/Module